Chapter 1

JOSEPHSON JUNCTION MATERIALS RESEARCH USING PHASE QUBITS

R. W. Simmonds[1], D. A. Hite[1,2], R. McDermott[1,3], M. Steffen[1,3], K. B. Cooper[1,3], K. M. Lang[1,4], John M. Martinis[1,3], D. P. Pappas[1]

[1]*National Institute of Standards and Technology*[*]*, 325 Broadway St. Boulder, CO 80305*
[2]*Physics Department, Western State College of Colorado, Gunnison, Colorado 81231*
[3]*Physics Department, University of California, Santa Barbara, CA 93106*
[4]*Physics Department, Colorado College, Colorado Springs, CO 80903*

Abstract At present, the performance of superconducting qubits is limited by decoherence. Strong decoherence of phase qubits is associated with spurious microwave resonators residing within the Josephson junction tunnel barrier [1]. In this work, we investigate three different fabrication techniques for producing tunnel junctions that vary the properties of the superconductor-insulator interface. Through experimental measurements, we characterize the junction and corresponding qubit quality. We find that there is a strong correlation between the morphology of oxidized base electrodes and the lowering of subgap currents in the junction I-V characteristics, while there is no noticeable improvement in the performance of fabricated phase qubits. Thus, "traditional" indicators of junction performance may not be enough to determine qubit performance. However, truly crystalline insulating barriers may be the key to improving Josephson junction based qubits.

Keywords: decoherence, Josephson tunnel junction, materials research, quantum computing.

1. Introduction

The most significant obstacle to the realization of a practical superconducting quantum computer is decoherence. We have found that the "quality" of Josephson junctions strongly affects the coherent performance of Josephson phase qubits [1]. Specifically, we have discovered spurious resonant states that couple to phase qubits, causing decoherence. In fact, there is evidence that all Josephson junction-based qubits might be suffering from these material defects [2]. Here we report measurements that show that by changing

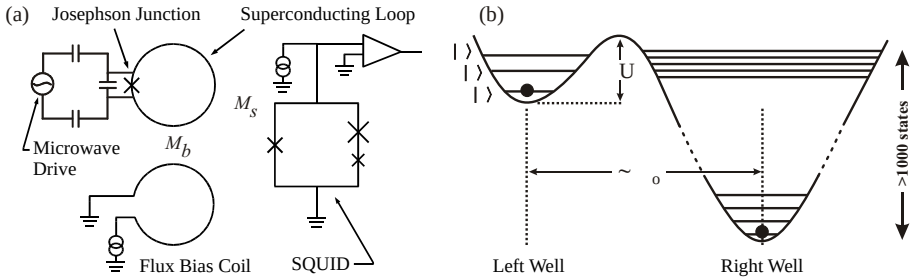

Figure 1.1. (a) The phase qubit schematic circuit. (b) The potential $U(\delta)$ at a particular ϕ.

the processing of fabricated tunnel junctions, in particular, through epitaxially grown base electrodes, one can improve the "traditional" indicators of Josephson tunnel junction performance, such as low subgap conductance. Although we find considerable improvement in the subgap currents, there is no noticeable improvement in the performance of fabricated phase qubits. This shows that "traditional" indicators of junction performance may not be enough to determine qubit performance. Furthermore, changing the properties of the superconductor-insulator interface, while still using amorphous barriers, does not significantly improve qubit performance. These results motivate the study of tunnel junctions formed by crystalline insulating barriers, which may be the key component in producing superconducting qubits of high quality.

2. Josephson Phase Qubits

We have developed a high-impedance current bias and measurement scheme for controlling a Josphson phase qubit, while providing sufficient isolation from the external environment. We include a Josephson junction in a superconducting loop of inductance L, as shown in Figure 1.1(a) and described in more detail elsewhere [1]. Microwave current lines are capacitively coupled to the junction, while a dc bias coil is placed some distance from the "qubit loop". For an applied flux $\phi = \Phi/\Phi_o$, where $\Phi_o = h/2e$ is the flux quantum, the potential energy $U(\delta)$ stored in the Josephson junction as a function of the superconducting phase difference δ is

$$U(\delta) = -\frac{\Phi_o}{2\pi} I_o \cos(\delta) + \frac{\Phi_o^2}{2L}(\phi - \frac{\delta}{2\pi})^2 \tag{2.1}$$

As shown in Figure 1.1(b), ϕ is chosen so that the qubit states, $|0\rangle$ and $|1\rangle$, are formed in the left ($\sim$cubic) well and the $|1\rangle$ state is measured by an induced tunneling event to states in the ($\sim$quadratic) right well, changing the flux in the qubit loop by roughly a flux quantum. This large flux difference allows for easy readout using a pulsed dc SQUID.

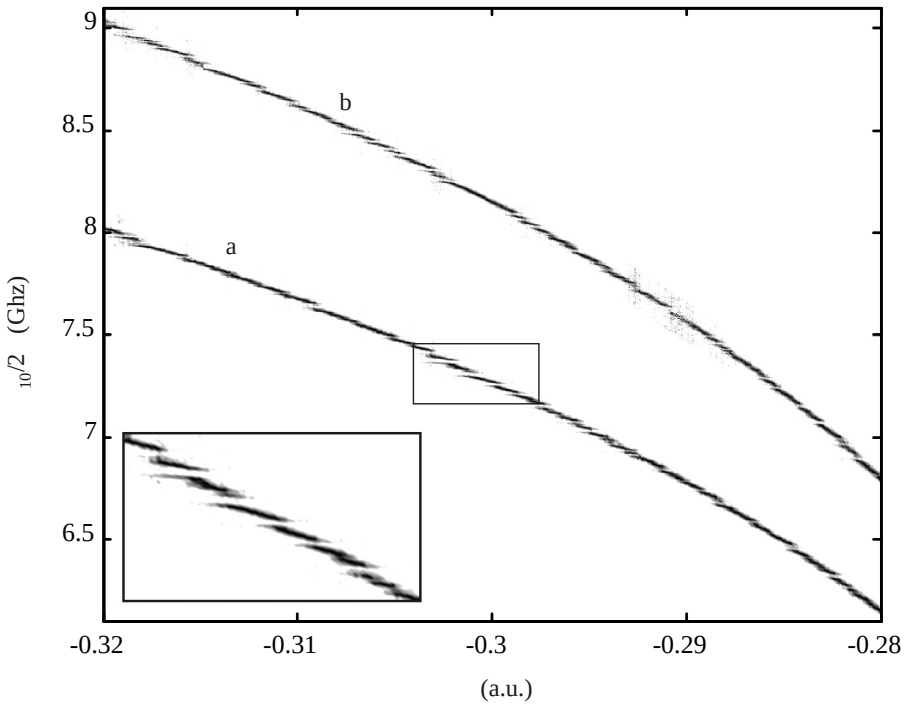

Figure 1.2. Qubit spectroscopy for of (a) a "ion mill process" qubit and (b) a "standard trilayer process" qubit.

The $0 \rightarrow 1$ qubit transition frequency ω_{10} is measured spectroscopically[3] by applying a microwave drive current $I_{\mu w}$ at frequency ω and subsequently measuring the occupation probability of state $|1\rangle$ using a "fast" qubit state measurement technique [4]. This is done for a range of static flux biases ϕ applied to the qubit loop. We observe in Figure 1.2 the expected decrease in the transition frequency as the current through the junction approaches the critical current. We also observe spurious resonators that are characteristic of energy level repulsion predicted for quantum mechanically coupled systems (see the inset of Figure 1.2). These extra resonators have a distribution in splitting size and frequency. They are indicative of nanoscopic two-level systems within the junction's insulating barrier. Away from any spurious resonators, we have observed coherent Rabi oscillations between the $|0\rangle$ and $|1\rangle$ state[1], while near a spurious resonator, we have found undesirable coupled interactions between the qubit and the resonator [4]. These resonators can be connected with measurements of the tunnel junction current-voltage (I-V) characteristic as discussed in Section 4.

3. Junction Fabrication Processes

State-of-the-art Josephson junctions employing superconducting (Al or Nb) electrodes and native-oxide tunnel barriers are typically fabricated using sputter deposition onto thermally oxidized Si wafers. For most applications, such as SQUID technologies, there has never been a necessity to improve the crystalline quality of the junction to correspondingly improve the device performance [5]. However, the discovery of spurious high-frequency resonant states within Josephson tunnel barriers, which are undesirable defects for quantum computing applications, suggests that more effort should be employed in order to improve junction fabrication. Here, we detail recent efforts to improve Josephson junction "quality" through different fabrication techniques. Ultimately, we would like to test whether the crystalline quality in the microstructure of the junctions correlates to improved low-frequency transport measurements, lower levels of 1/f critical current noise, and finally, qubit performance.

In what follows, the "ion mill" and "sputtered trilayer" junctions are produced on 3-inch thermally oxidized Si(100) wafers in our clean room sputter chamber with a base pressure of 7×10^{-8} Torr, while the "evaporated trilayers" are deposited in a UHV chamber with base pressure 8×10^{-11} Torr on Si(111) chips, 2.5×2.5 cm^2. The Al films are grown by dc magnetron sputter deposition using 5 mTorr Ar with the substrate at room temperature. The oxidation parameters are typically 10 Torr of oxygen pressure for a 10 min exposure at room temperature. This procedure leads to the preferred oxide thickness, giving junction critical-current densities of $\sim 15 - 20$ A/cm^2, appropriate for our phase qubits. The base electrodes for all devices discussed here have a thickness of 200 nm, while the top Al films are from 60 to 200 nm thick.

3.1 The "Ion Mill Junction Process"

The "ion mill process" (IMP) for Josephson junction fabrication[6], as shown in Figure 1.3(a), is a simple and convenient method for producing tunnel junctions. We begin by sputtering a base Al wiring layer, which is then defined using a wet acid etch. This surface is then covered with ~ 350 nm of SiO_2 for

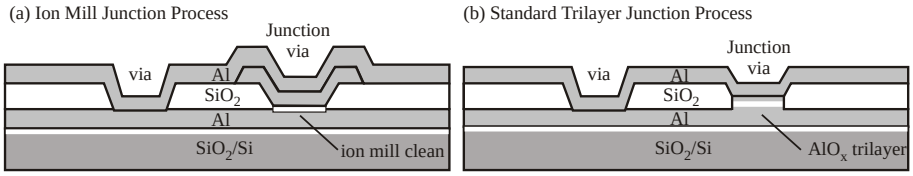

Figure 1.3. The (a) ion mill process (IMP) and (b) standard trilayer process (STP) for producing Josephson tunnel junctions.

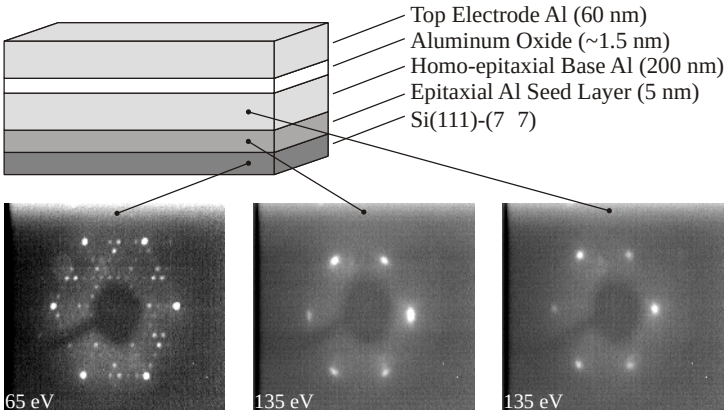

Figure 1.4. Schematic diagram of different layers in the $Al/AlO_x/Al/Si(111)$ evaporated trilayer growth sequence. The LEED images show the quality of the epitaxial seed layer and the base electrode. The LEED images were obtained with electron energies of 65 eV, 135 eV, and 135 eV respectively. The oxide film and top electrode are amorphous.

insulation. We define the area of the tunnel barrier by etching a via through the SiO_2. After breaking vacuum, the native oxide on this exposed surface is then removed from the base electrode by ion milling at 800 V with 0.1 mA/cm^2 for 1 minute (creating an atomically *rough* surface), and the amorphous tunnel barrier is grown by thermal oxidation at room temperature. Following oxide growth, a fresh layer of Al is deposited to form the tunnel junction. Most of this layer is then wet etched away except for an area defining the junction. Subsequent SiO_2 etching, ion milling, and deposition steps define vias for contacting to the base wiring layer and the tunnel junction.

3.2 The “Standard Trilayer Junction Process"

We have developed a “standard trilayer process” (STP) that produces tunnel junctions with superconductor-insulator interfaces that are smoother than the IMP junctions. As shown in Figure 1.3(b), the oxide tunnel barrier is grown *in situ* on a freshly sputtered Al base layer without breaking vacuum, then the tunnel barrier is immediately capped with another sputtered Al layer. The Josephson junction area is defined by ion milling the top two layers of the trilayer to create a mesa. The base wiring layer is then defined using a wet etch. This surface is then covered with $\sim$ 350 nm of SiO_2 for insulation. Subsequent processing steps define vias for electrical contacts between the top wiring layer, the trilayer junction, and the bottom wiring layer.

3.3 The “Evaporated Trilayer Junction Process"

The “evaporated trilayer process” (ETP) grows Josephson junctions in a unique way using advanced growth techniques in order to produce atomically smooth superconductor-insulator interfaces with fewer structural defects. Typically, metal films grown on semiconductor surfaces follow a three-dimensional growth mode. It is often found that interdiffusion and reactive epitaxy dominate in the early stages of growth for many metal-on-semiconductor systems. This results in further clustering and hinders the production of smooth films and abrupt interfaces. Sputter deposition used for the STP junctions can produce Al films with lower rms roughness; however, due to high deposition rates and kinetic limitations, these films are dominated by crystal defects and are polycrystalline at best.

Here, we use clean Si(111) substrates, flash anneal them at 1500 K, and use standard cleaning procedures[7] to obtain a (7×7) reconstructed surface. We use this surface because it is clean, highly ordered, thermodynamically stable, and allows the epitaxial growth of Al [8]. Furthermore, it has been shown that low-temperature deposition of Al on Si(111)-(7×7), followed by annealing, produces films with extremely sharp and very well defined surfaces [9]. This is in contrast to films grown under room-temperature conditions [10], but consistent with the novel growth mechanisms responsible for atomically flat metal films on semiconductor substrates [11].

We start by evaporating an epitaxial Al seed layer (~ 5 nm thick) on the Si(111)-(7×7) surface, held at 120 K during deposition and subsequently annealed at 475 K. We have used low-energy electron diffraction (LEED) to determine the crystalline quality of the substrate, seed layer, and subsequent films. Once the Al seed layer is prepared, we then complete the base electrode through the homoepitaxy of Al on the seed layer at room temperature. Although this base electrode is 200 nm thick, Figure 1.4(c) shows that it still exhibits a LEED pattern of fairly high quality. The evaporated trilayer is then completed by thermal oxidation at room temperature, followed by evaporation of the final top electrode. Each step of the growth was monitored with Auger electron spectroscopy (AES), and LEED. After the oxidation there was no LEED pattern to report, as expected, due to the amorphous nature of the native oxide. AES data indicated clean metal films with no detectable amounts of contaminants. In addition, *ex situ* atomic force microscopy (AFM) measurements have indicated smoother oxides when compared to surfaces produced after sputter deposition, and significantly smoother than those evaporated onto non-epitaxial substrates. The subsequent steps for producing devices from the ETP are the same as those described above for the STP.

4. Josephson Junction and Qubit Characterization

We interpret I-V curves for tunnel junctions in the context of the Landauer tunneling model[12, 13] for junction conductance. The conductance G of tunnel junctions at voltages above the superconducting gap voltage ($2\Delta/e$) is expressed as a sum over the individual conductance channels, $G = G_o \sum_{i=1}^{N} \tau_i$, where $G_o = 2e^2/h$ and τ_i is the transmission probability of the ith channel. At low voltages, nth-order multiple Andreev reflections form steps in the quasiparticle branch of the I-V characteristic of magnitude $2/\tau_i$. If we assume the current is carried by N channels, each with an average transmission τ, then the largest step appearing in the I-V characteristic is given by $\sim 2/\tau$. We imagine that these individual channels fluctuate "on" and "off" as switches, so that the average size of a critical-current fluctuation is $\delta I_o \approx 2\Delta G_o \tau/e$. If the two level resonators in the tunnel barrier couple to the qubit through the critical current, then the size of each resonant level splitting is directly proportional to δI_o. By correlating measurements of the subgap conductance from I-V characteristics (Section 4.1 below) and qubit spectroscopy (Section 2) we find the relationship between what has traditionally been considered "high quality" Josephson junctions[14] and the corresponding quality of phase qubits.

4.1 Measurements of Junction I-V Characteristics

For direct comparison, all samples are processed into hysteretic tunnel junctions (of the type used in phase qubits with $\beta_c \gg 1$) through standard photolithographic techniques. The I-V characteristics of the junctions are measured[1] at temperatures below 50 mK. I-V characteristics from IMP, STP, and ETP junctions are shown in Figure 1.5. Each curve has been normalized by its critical current I_o in order to facilitate a relative comparison of subgap currents. The I-V from the STP junction shows a current step size at $2\Delta/e \approx 380\mu$V which is roughly larger by a factor of 6 than for the IMP junction. Even more pronounced is the ETP junction, whose subgap currents are lower still by almost another order of magnitude. The reduced subgap current of the STP and ETP junctions indicates a relatively large number of conduction channels, each with relatively low transmissivity. However, the distribution of τ_i's, which can fluctuate at GHz frequencies, may or may not be contributing strongly to the measured, average τ. If their influence *did* strongly determine τ, then we would expect that the fluctuation of the junction critical current due to these

[1] We use a nonlinear current bias made from diodes and resistors in order first to exceed the critical current, then to sample more densely quasiparticle currents, smaller by several orders of magnitude, in the subgap region. To ensure that the features of the I-V characteristic are not distorted by high-frequency interference, these measurements were performed using RC low-pass filters cooled at 4 K.

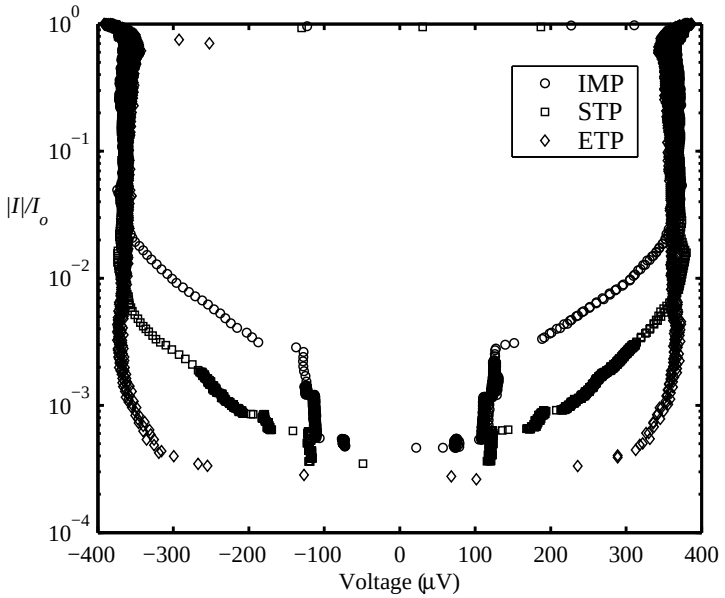

Figure 1.5. I-V characteristics, normalized current $|I|/I_o$ vs. voltage, for tunnel junctions with area $\sim 70\ \mu\text{m}^2$ comparing the IMP ($I_o \sim 20\ \mu$A), STP ($I_o \sim 10\ \mu$A), and ETP ($I_o \sim 10\ \mu$A).

resonant channels will be reduced, so that the maximum level splitting size found in spectroscopy data for trilayer qubits should be reduced. This would then allow us to predict the quality of superconducting qubits through a "traditional" quality check of just the Josephson tunnel junctions themselves (and there is a vast amount of this information in the current literature for different Josephson junction technologies).

4.2 Measurements of Qubit Spectroscopy

In Figure 1.2, we show two samples of spectroscopic data from two qubits with the exact same geometrical design but with IMP and STP junctions used in each respective device.[2] In Figure 1.5, the I-V characteristics show a difference of almost an order of magnitude in the subgap conductance for these two junction fabrication methods. From a "traditional" point of view, the trilayer junctions are considered "higher quality" junctions. However, spectroscopic characterization of the phase qubits, as seen in Figure 1.2, shows *no* signifi-

[2] Unfortunately, thus far, we have not been able to compare qubit spectroscopy results for the ETP junctions because of low junction yield over a single chip. However, we have tested numerous STP qubits and three similar IMP qubits.

cant difference in the maximum level splitting amplitude or in the number of resonators per frequency range. Furthermore, measurements of the $|1\rangle$ state energy relaxation time ($\sim$ 400 ns), the Rabi oscillation visibility ($\sim 50\%$), and the Rabi oscillation decay time ($\sim$ 80 ns) were typical for both types of qubits. This suggests, if our microscopic model is still correct, that the number of high-frequency resonators that we see in the spectroscopy, which are very few compared to the total number of resonators including those at very low frequency, do not contribute significantly to the properties of the measured I-V characteristic. Thus, our "traditional" notions of junction quality obtained through low-frequency measurements are not sufficient for characterizing the quality of Josephson phase qubits operated at GHz frequencies. These spectroscopic measurements are crucial for identifying defects not seen using standard low-frequency techniques.

5. Concluding Remarks

We have grown superconducting tunnel junctions using three different processing techniques: IMP, STP, and ETP. The last uses an atomically flat metallic seed layer of Al on Si(111)-(7×7) substrates in order to produce an epitaxial base electrode with an atomically smooth interface. Tests junctions were fabricated using all three techniques, while qubits were successfully produced using the first two processing techniques (IMP and STP). Low-frequency transport measurements (I-V characteristics) as well as high-frequency measurements (qubit spectroscopy) were made below 50 mK. I-V characteristics for all three samples have been compared and we conclude that there is a strong correlation between the morphology of atomically smooth thermally oxidized base electrodes and the lowering of subgap currents. However, for the first two processing techniques (IMP and STP), qubit measurements showed that these "traditional" indicators did not assure the fabrication of high-quality Josephson phase qubits. Future tests will focus on the crystalline quality of the insulating barrier itself. This may play the pivotal role in eliminating spurious resonators in tunnel junctions and producing high-quality superconducting quantum bits.

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